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		REPRENTATIVE DIVISION ENGINEERING DEPARTMENT 2 DUTYPANEL DEVELOPMENT CENTER NARA LIQUID CRYSTAL DISPLAY GROUP
	SPECIFICATION	

DEVICE SPECIFICATION for

PassiveMatrix COLOR LCD Module
(300x600 dots)

Model No.

LM80C20PX

❑ ICUSTOHER'S APPROVAL

BY _____

PREESENTED
BY Y. Inoue

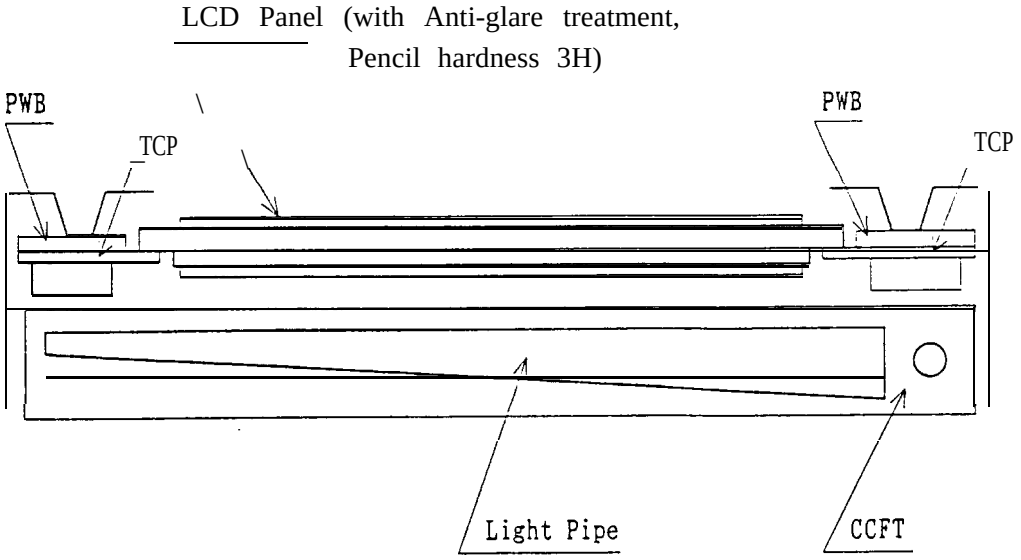
Y. Inoue
DEPARTMENT GENERAL MANAGER
ENGINEERING DEPARTMENT II
DUTY PANEL DEVELOPMENT CENTER
LIQUID CRYSTAL DISPLAY GROUP
SHARP CORPORATION

1. Application

This data sheet is to introduce the specification of LM80C20PX, Passive Matrix type Color LCD Module.

2. Construction and Outline

Construction: 800x600 dots color display Module consisting of an LCD panel, PWB(printed wiring board) with electric components mounted onto, TCP(tape carrier package) to connect the LCD panel and PWB electrically, and plastic chassis with CCFT back light and bezel to fix them mechanically.
Signalground(VSS)is connected with the metal bezel.
DC/DC converter is built in.



Outline : See Fig. 10
Connection : See Fig. 10 and Table 6

3. Mechanical Specifications

Table 1

Parameter	Specifications	Unit
Outline dimensions	264.5±0.5(W)×193.5±0.5(H) x8.5max.	mm
Active Area	230.375(W) X172.775(H)	mm
Display format	800(W) X600(H) full dots	—
Dot size	0.071×RGB(W)X0.263(H)	mm
Dot spacing	0.025	mm
*1 Base color	Normally black *2	—
Weight	Approx. 420	g

*1 Due to the characteristics of the LC material, the colors vary with environmental temperature.

*2 Negative-type display
Display data "H" : ON → transmission
Display data "L": OFF → light isolation

4. Absolute Maximum Ratings

4-1 Electrical absolute maximum ratings

Table 2

Parameter	Symbo 1	MIN.	MAX.	Unit	Remark
Supply voltage (Logic)	V_{DD}-V_{SS}	o	6.0	v	Ta=25 "C
Input voltage	V_{IN}	0.3	V_{DD}+0.3	v	Ta=25 "C

4-2 Environmental Conditions

Table 3

Item	Tstg		Topr		Remark
	MIN.	MAX.	MIN.	MAX.	
Ambient temperatuer	-25 "C	+60 "C	0 "C	+40 "C	Note 4)
Humidity	Note 1)		Note 1)		No condensation
Vibration	Note 2)		Note 2)		3 directions (X/Y/Z)
Shock	Note 3)		Note 3)		6 directions (±X±Y±Z)

Note 1) Ta≦40 'C . . . . .80% RH Max

Ta>40 'C . . . . .Absolute humidity shall be less than Ta=40°C/80% RH.

Note 2)

Table 4

Frequency	IOH, ~57 Hz	58 Hz ~500 Hz
Vibration level	—	9.8 m/s²
Vibration width	0.075 mm	l - l
Interval	10 Hz ~500 Hz ~10 Hz/11.0 mi	

2 hours for each direction of X/Y/Z (6 hours as total)

Note 3) Accerelation : 490 m/s²

Pulse width : 11 ms

3 times for each direction o ±X/±Y/±Z

Note 4) Care should be taken so that the LCD Module may not be subjected to the temperature out of this spec fication.

5. Electrical Specifications

5-1 Electrical characteristics

Ta=25 °C, V_{DD}=5 V±10 %

Table 5 (1/tFRM= 120 Hz)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage (Logic)	V_{DD}-V_{SS}	Ta=0～40°C	4.5	5.0	5.5	V
Contrast adjust voltage	Vcon-V_{SS}	Ta=0～40°C Note 4) 5)	1.0	1.95	2.5	V
Input signal voltage	V_{IN}	'H' level	2.0	—	V_{DD}+0.3	V
		'L' level	-0.3	—	0.8	V
Input leakage current	I_{IL}	'H' level	—	—	1.0	μA
		'L' level	-1.0	—	—	μA
Supply current (Logic)	I_{DD} (Typ)	Note 2),	—	85	120	mA
	I_{DD} (Max)	Note 3),	—	315	410	mA
Rush Current (Logic)	Irush	Ta=25 °C, Power On 3 A(pk)×20 ms+1 A(pk)×10 μs(max)				
Power consumption	Pd (Typ)	Note 2),	—	425	600	mW
	Pd (Max)	Note 3),	—	1 575	2 050	mW

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply current (Logic)	I_{DD} (Typ)	Note 2),	—	65	100	mA
	I_{DD} (Max)	Note 3),	—	210	300	mA
Power consumption	Pd (Typ)	Note 2),	—	325	500	mW
	Pd (Max)	Note 3),	—	1 050	1 500	mW

Note 1) Under the following conditions.;

①Immediately after the rise of DISP signal. : 3.0 A × 20 ms

②Under the situation that DISP signal is on and kept steady. : 1.0 A × 10 μs

Note 2) Under the following conditions.;

Vcon-Vss : contrast max. (Vcon=1.95 V :120 Hz Vcon=2.55 V :73 Hz)

V_{DD}-Vss=5.0 ± 0.3V

Frame requency = 120 (73) Hz

Displa pattern = white stripe pattern.

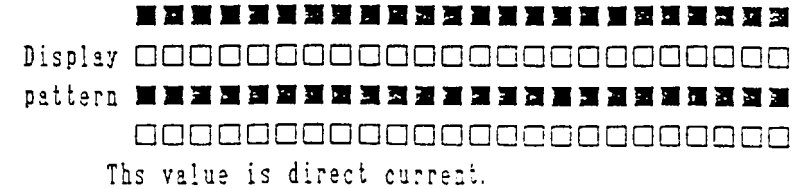
Note 3) Under the following conditions.;

Vcon-Vss : contrast max. (Vcon=1.95 V :120 Hz, Vcon=2.55 V :73 Hz

V_{DD}-Vss=5.0 ± 0.3V

Frame requency = 120 (73] Hz

Displa pattern = black/white stripe pattern.

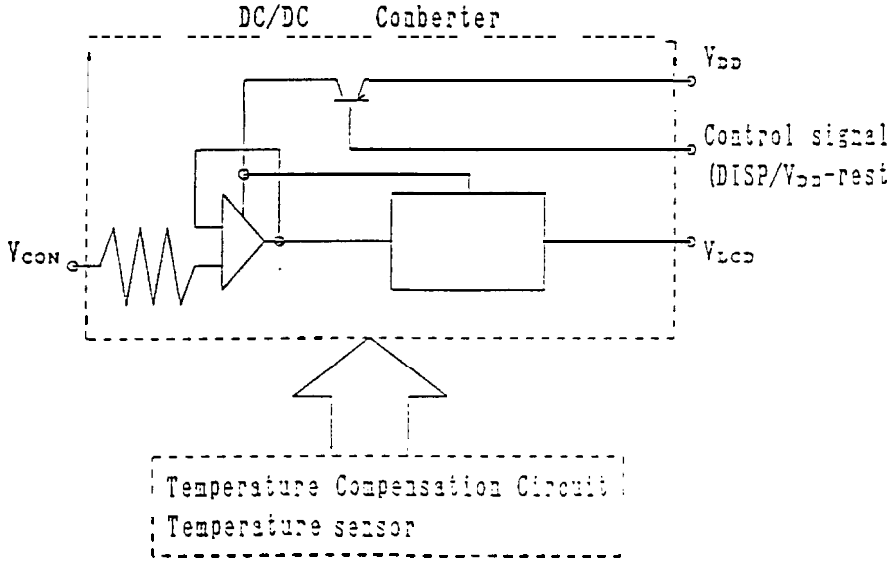


Ths value is direct current.

Note 4)

Contrast adjustment voltage 'Vcon-Vss' is transformed into the LCD driving voltage 'V_{LCD}' by following circuit built in the LCD module.

LCD driving voltage 'V_{LCD}' is adjusted automatically according to the change of ambient temperature range by the temperature compensation circuit.



Note 5)

Temperature compensation circuit built in LCD module have been set obtain the optimum contrast under following driving condition ;

Take care that voltage for optimum contrast is changed under the different condition.

Frame frequency : 120 Hz, Duty ratio : 300 (an odd number frame), Ta= 25 °C
328 (an even number frame)

※ Electrical and optical characteristics are specified by above condition.

○LCD

Table 6

Pin No.	Symbol	Function	Remark
1	VSS	Ground potential	—
2	XCK	Data input clock signal	"H"—"L"
3	VSS	Ground potential	—
4	VSS	Ground potential	—
5	LP	Input data latch signal	"H"—"L"
6	YD	Scan start-up signal	"H"
7	VSS	Ground potential	—
8	VSS	Ground potential	—
9	VDD	Power supply for logic and LCD (+5V)	—
10	DISP	Display control signal	H(ON), L(OFF)
11	VSS	Ground potential	—
12	VSS	Ground potential	—
13	VSS	Ground potential	—
14	DL7	Display data signal (Lower)	H(ON), L(OFF)
15	DL6	Display data signal (Lower)	H(ON), L(OFF)
16	DL5	Display data signal (Lower)	H(ON), L(OFF)
17	DL4	Display data signal (Lower)	H(ON), L(OFF)
18	DL3	Display data signal (Lower)	H(ON), L(OFF)
19	DL2	Display data signal (Lower)	H(ON), L(OFF)
20	DL1	Display data signal (Lower)	H(ON), L(OFF)
21	DL0	Display data signal (Lower)	H(ON), L(OFF)
22	VSS	Ground potential	—
23	VSS	Ground potential	—
24	VSS	Ground potential	—
25	DU0	Display data signal (Upper)	H(ON), L(OFF)
26	DU1	Display data signal (Upper)	H(ON), L(OFF)
27	DU2	Display data signal (Upper)	H(ON), L(OFF)
28	DU3	Display data signal (Upper)	H(ON), L(OFF)
29	DU4	Display data signal (Upper)	H(ON), L(OFF)
30	DU5	Display data signal (Upper)	H(ON), L(OFF)
31	DU6	Display data signal (Upper)	H(ON), L(OFF)
32	DU7	Display data signal (Upper)	H(ON), L(OFF)
33	VSS	Ground potential	—
34	VSS	Ground potential	—
35	VSS	Ground potential	—
36	VDD	Power supply for logic and LCD (+5V)	—
37	VDD	Power supply for logic and LCD (+5V)	—
38	VCON	Contrast adjust voltage	—
39	NC	—	—
40	VSS	Ground potential	—
41	VSS	Ground potential	—

○CCFT

Pin No	Symbol	Description	Level
1	HV	High voltage lineal (from Inverter)	—
2	NC	—	—
3	GND	Ground line (from Inverter)	—

NOTE) Pin No. and its location are shown in Fig

OLCD

Used connector:DF9B-41P-1V (HIROSE)

Mating connector: DF9B-41S-1V (HIROSE)

○CCFT

Used connector : BHR-03VS-1 (JST)

Mating connector:SM03(4.0)B-BHS or SM02(8.0)B-BHS(JST)

Except above connector shall be out of guaranty

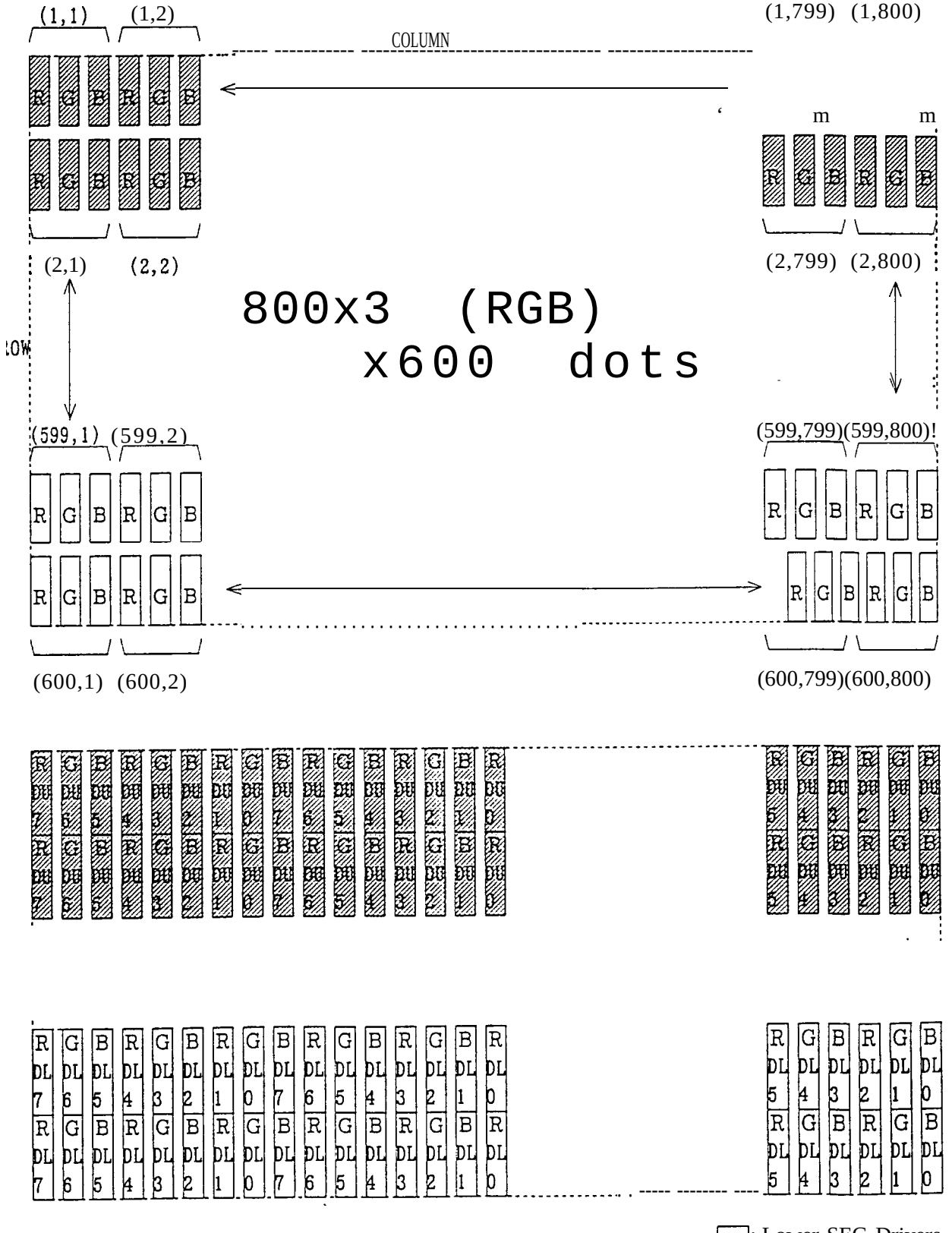


Fig.1 Dot chart of display area

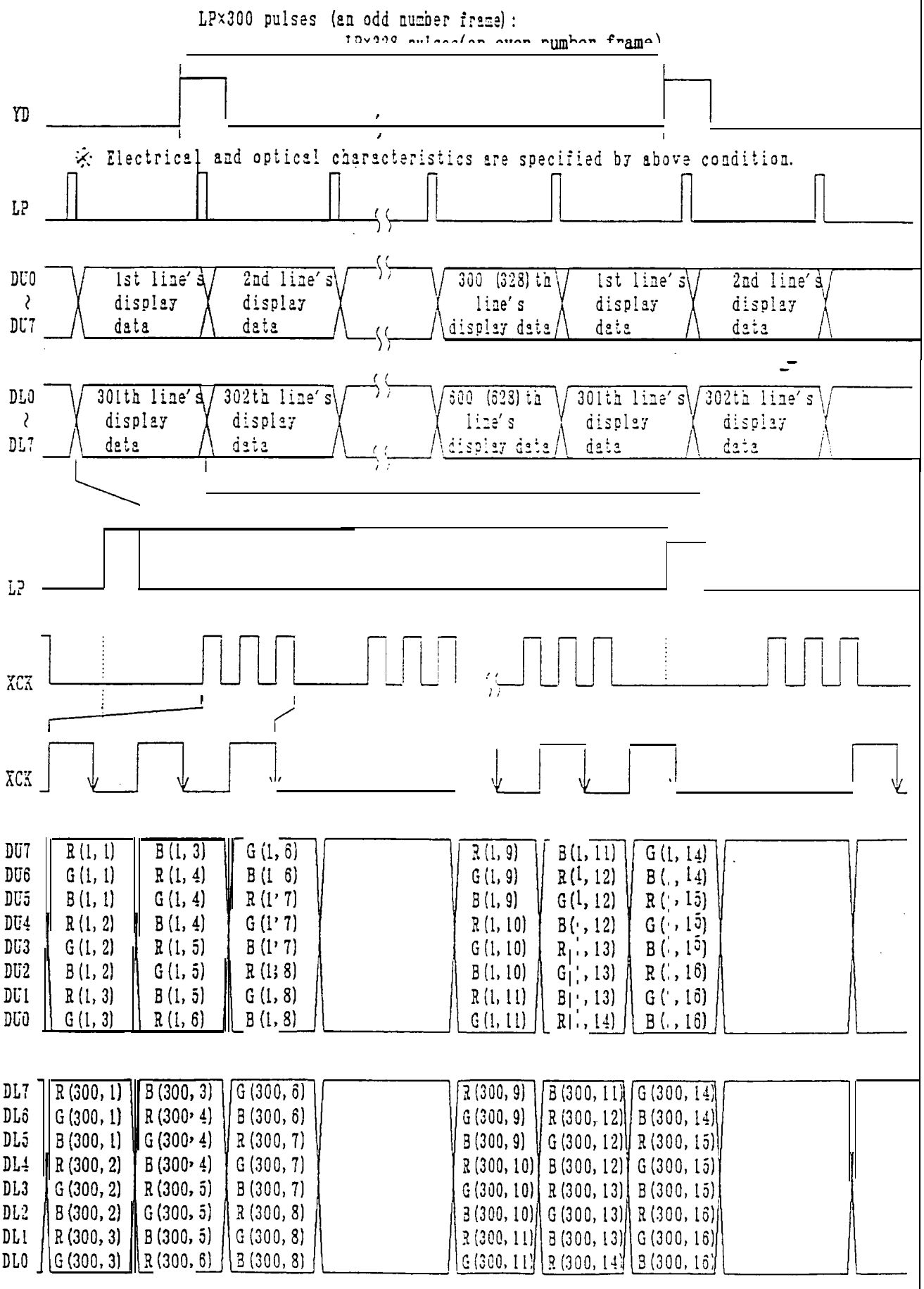


Fig. 2 Data input timing chart

Table 7 Interface timing ratings

Item	Symbol	Rating MIN.	TYP.	MAX.	Unit
Frame cycle	tFRM	※ 8.3		16.94	ms
YD signal 'H' level set up time	tHYS	100			ns
"H" level hold time	tHYH	100			ns
'L' level set up time	tLYS	100			ns
'L' level hold time	tLYH	40			ns
LP signal 'H' level pulse width	tWLPH	200			ns
XCK signal clock cycle	tCK	※ 50			ns
'H' level clock width	tWCKH	※ 27			ns
'L' level clock width	tWCKL	※ 15			ns
Data set up time	tDS	※ 21			ns
hold time	tDH	※ 17			ns
LP↑ allowance time from XCK↓	tLS	200			ns
XCK↑ allowance time from LP↓	tLH	200			ns
Input signal rise/fall time	tr, tf			13	ns

※ The intervals one LP fall and the next must be always the same, and LPs must be input continuously.
The interval must be 70μs Max.

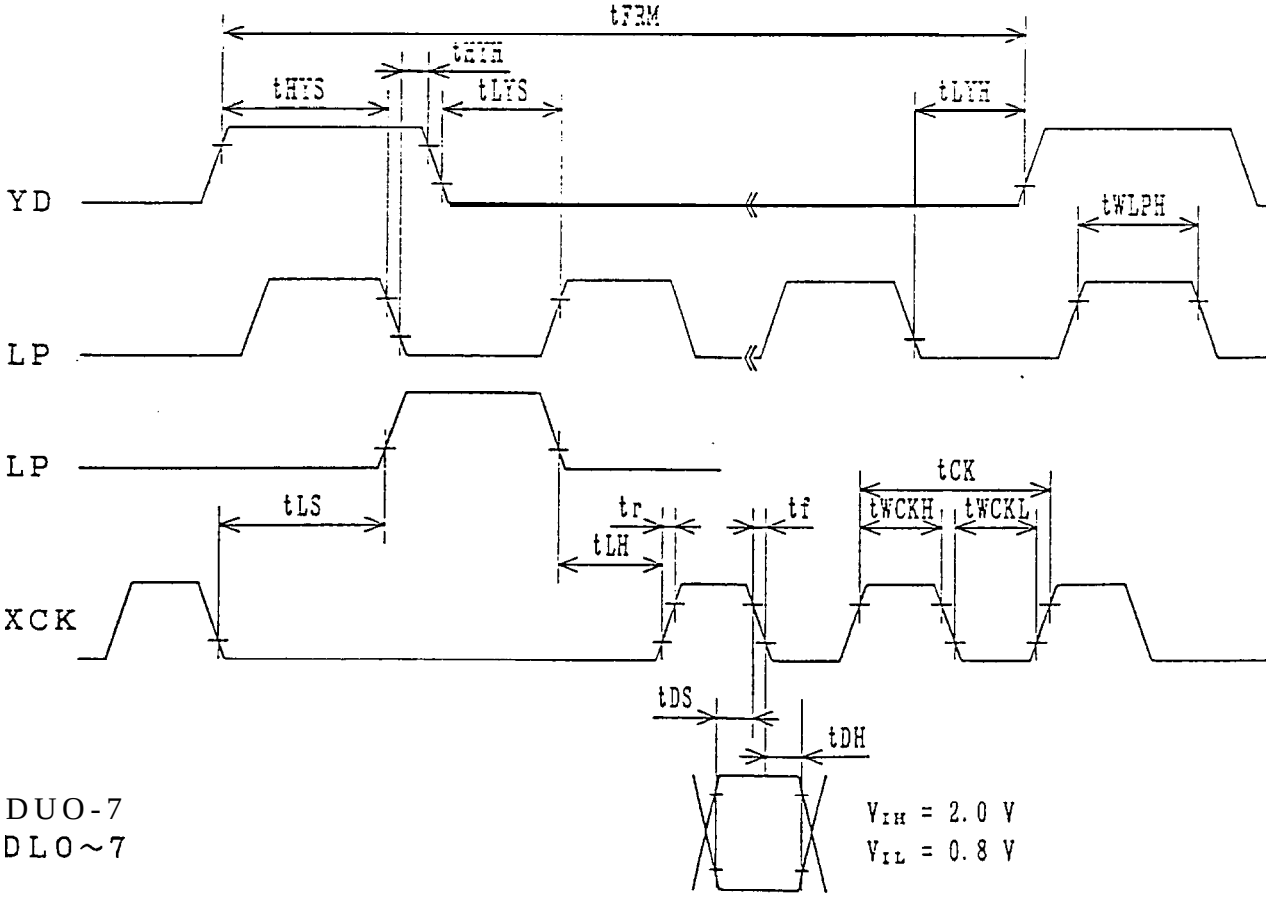


Fig.3 Interface timing chart

6. Module Driving Method

6.1 Circuit configuration

Fig. 9 shows the block diagram of the module's circuitry.

6.2 Display Face Configuration

The display consists of 800×3 (R, G, B)×600 dots as shown in Fig. 1.
The interface is single panel with double drive to be driven at 1/300(328) duty ratio.
(300:an odd number frame, 328:an even number frame)

6.3 Input Data and Control Signal

The LCD driver is 240 bits LSI, consisting of shift registers, latch circuits and LCD driver circuits. Input data for each row (800×3 R, G, B) will be sequentially transferred in the form of 8 bit parallel data through shift registers from top left of the display together with clock signal (XCK).

When input of one row (800 × 3, R, G, B dots) is completed, the data will be latched in the form of parallel data corresponding to the signal electrodes by the falling edge of latch signal (LP). Then, the corresponding drive signals will be transmitted to the 800 × 3 lines of column electrodes of the LCD panel by the LCD drive circuits.

At this time, scan start-up signal (YD) has been transferred from the scan signal driver to the 1st row of scan electrodes, and the contents of the data signals are displayed on the 1st row of the display face according to the combinations of voltages applied to the scan and signal electrodes of the LCD. While the data of 1st row are being displayed, the data of 2nd row are entered. When data for 800×3 dots have been transferred, they will be latched by the falling edge of LP, switching the display to the 2nd row.

Such data input will be repeated up to the 300(328)th row of each display segment, from upper row to lower rows, to complete one frame of display by time sharing method.

Simultaneously the same scanning sequence occur at the lower panel.
Then data input proceeds to the next display frame.

YD generates scan signal to drive horizontal electrodes.

Since DC voltage, if applied to LCD panel, causes chemical reaction in LC materials, causing deterioration of the materials, drive wave-fern shall be inverted at every display frame to prevent the generation of such DC voltage. Control Signal M plays such a role.

Because of the characteristics of the CMOS driver LSI, the power consumption of the display module goes up with the clock frequency of XCK.
To minimize data transfer speed of XCK clock the LSI has the system of transferring 8 bit parallel data through the 8 lines of shift registers.
Thanks to this system the power consumption of the display module is minimized.

In this circuit configuration, 8 bit display data shall input to data input pins of DU0～7 and DL0～7.

Furthermore, the display module has bus line system for data input to minimize the power consumption with data input terminals of each driver LSI being activated only when relevant data input is fed.

Data input for column electrodes and chip select of driver LSI are made as follows:

The driver LSI at the left end of the display face is first selected, and the adjacent driver LSI right next side is selected when data of 240 dot (30XCK) is fed. This process is sequentially continued until data is fed to the driver LSI at the right end of the display face. This process is followed simultaneously both at the top and bottom column drivers LSI's.

Thus data input will be made through 8 bit bus line sequentially from the left end of the display face.

Since this display module contains no refresh RAM, it requires the above data and timing pulse inputs even for static d splay.

The timing chart of input signals are shown in Fig. 3 and Table 7.

7. Optical Characteristics

Ta = 25°C, V_{DD} = 5.0 V, Vcon-V_{SS} = Vmax

Table 8

Following spec are based upon the electrical measuring conditions, on which the contrast of perpendicular direction ($\theta x=\theta y=0°$) will be MAX.

Parameter		Symbol	Condition	MIN.	TYP.	MAX.	Unit	Remark
Viewing angle range		θx	Co>5.0 $\theta y=0°$	-30	-	30	dgr.	Note1)
		θy	$\theta x=0°$	-15	-	20	dgr.	
Contrast ratio		Co	$\theta x=\theta y=0°$	15	25	-		Note2)
Response time	Rise	τ r	$\theta x=\theta y=0°$	-	220	300	ms	Note3)
	Decay	τ d	$\theta x=\theta y=0°$	-	80	100	ms	
Unit chromaticity	White	x	$\theta x=\theta y=0°$	0.240	0.290	0.340	-	
		y	$\theta x=\theta y=0°$	0.280	0.320	0.380	-	

Note 1) The viewing angle range is defined as shown Fig. 4.

Note 2) Contrast ratio is defined as follows:

$$Co = \frac{\text{Luminance (brightness) all pixels 'White' at Vmax}}{\text{Luminance (brightness) all pixels 'dark' at Vmax}}$$

Vmax is defined in Fig. 6.

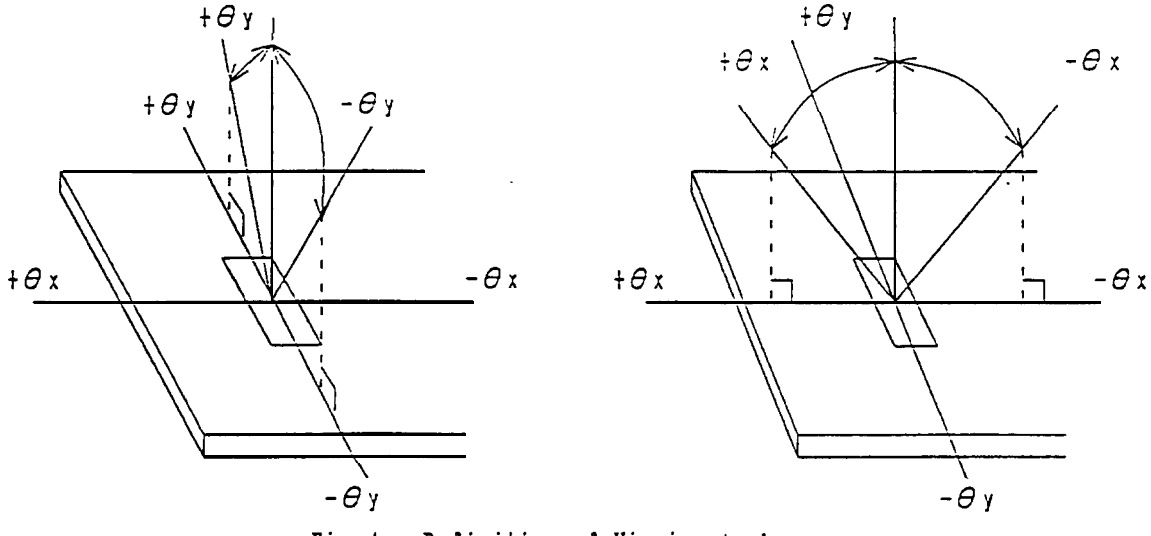
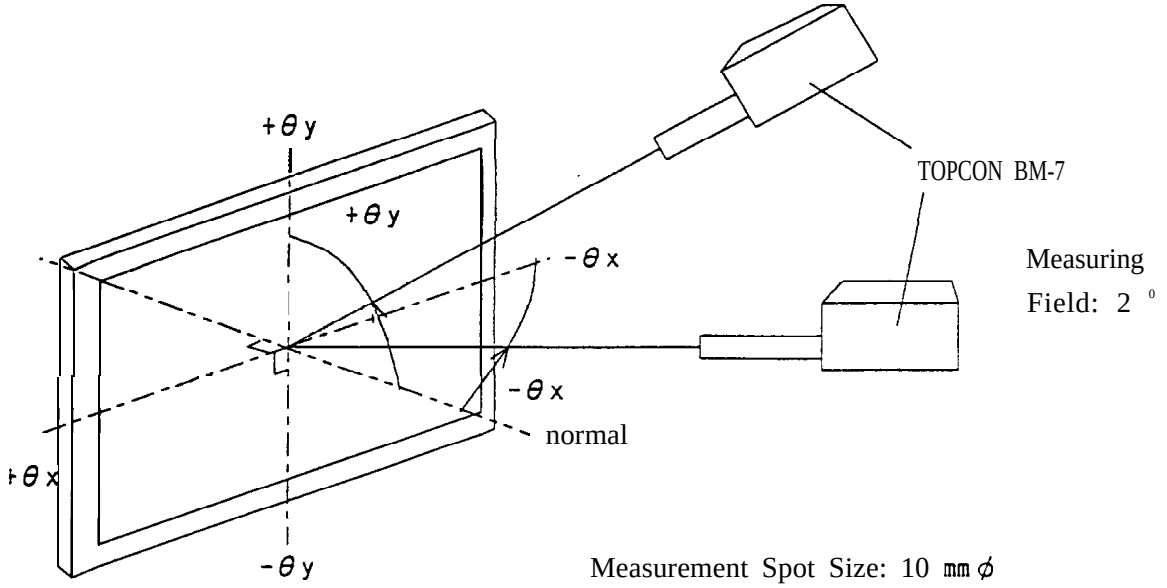


Fig. 4 Definition of Viewing Angle

Note 3] The response characteristics of photo-detector output are measured as shown in Fig. 7, assuming that input signals are applied so as to select and deselect the dots to be measured, in the optical characteristics test method shown in Fig. 8.



Measurement Spot Size: 10 mm ϕ

θx:Angle from "normal" to viewing surface roteted about the horizontal axis.

θy:Angle from "normal" to viewing surface roteted about the vertical axis.

Fig. 5 Optical Characteristics Test Method I

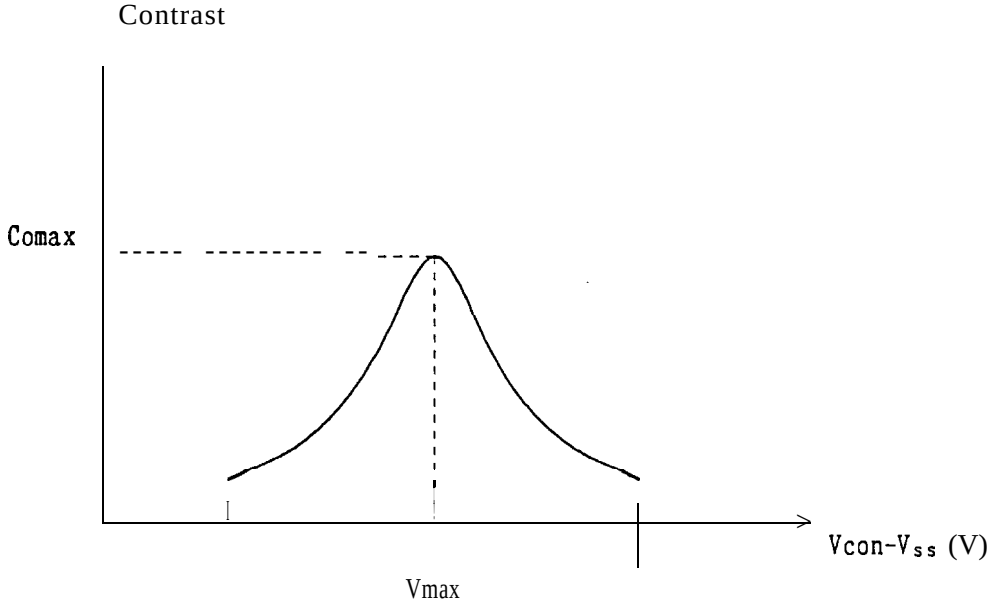


Fig. 6 Definition of V_{Max}

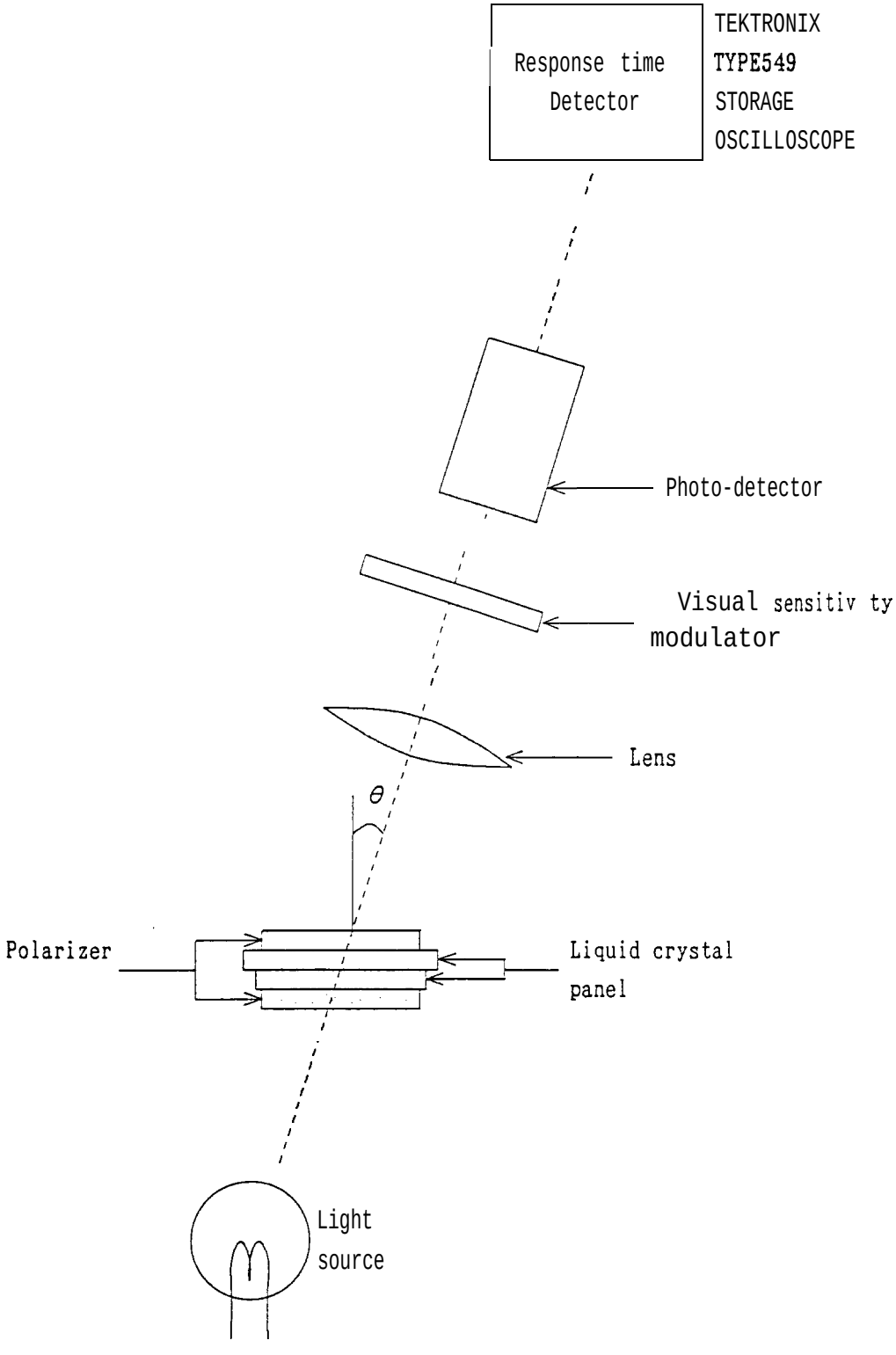
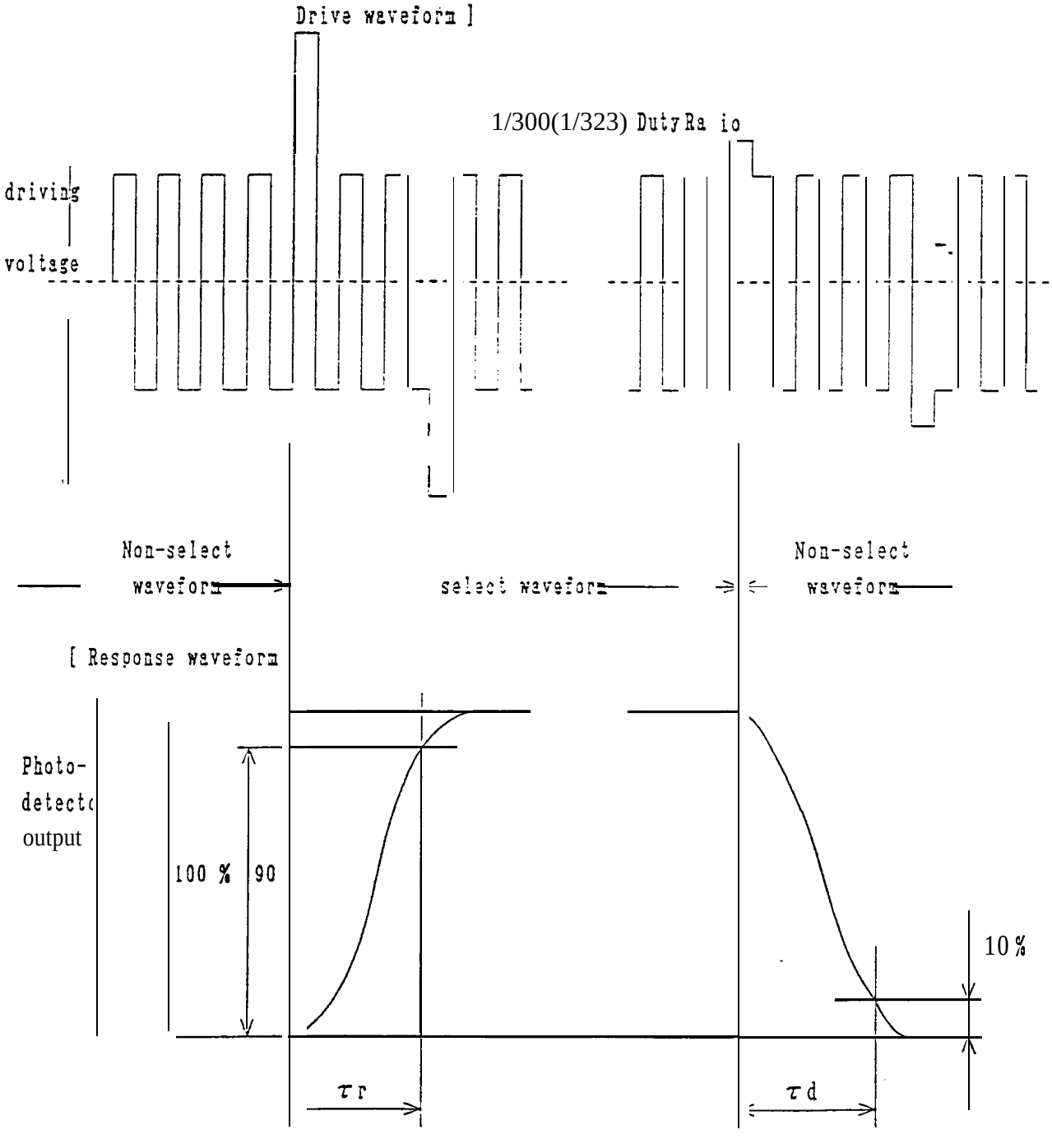


Fig.7 Optical Characteristics Test Method II



τr: Rise time
τd: Decay time

Fig. 8 Definition of Response Time

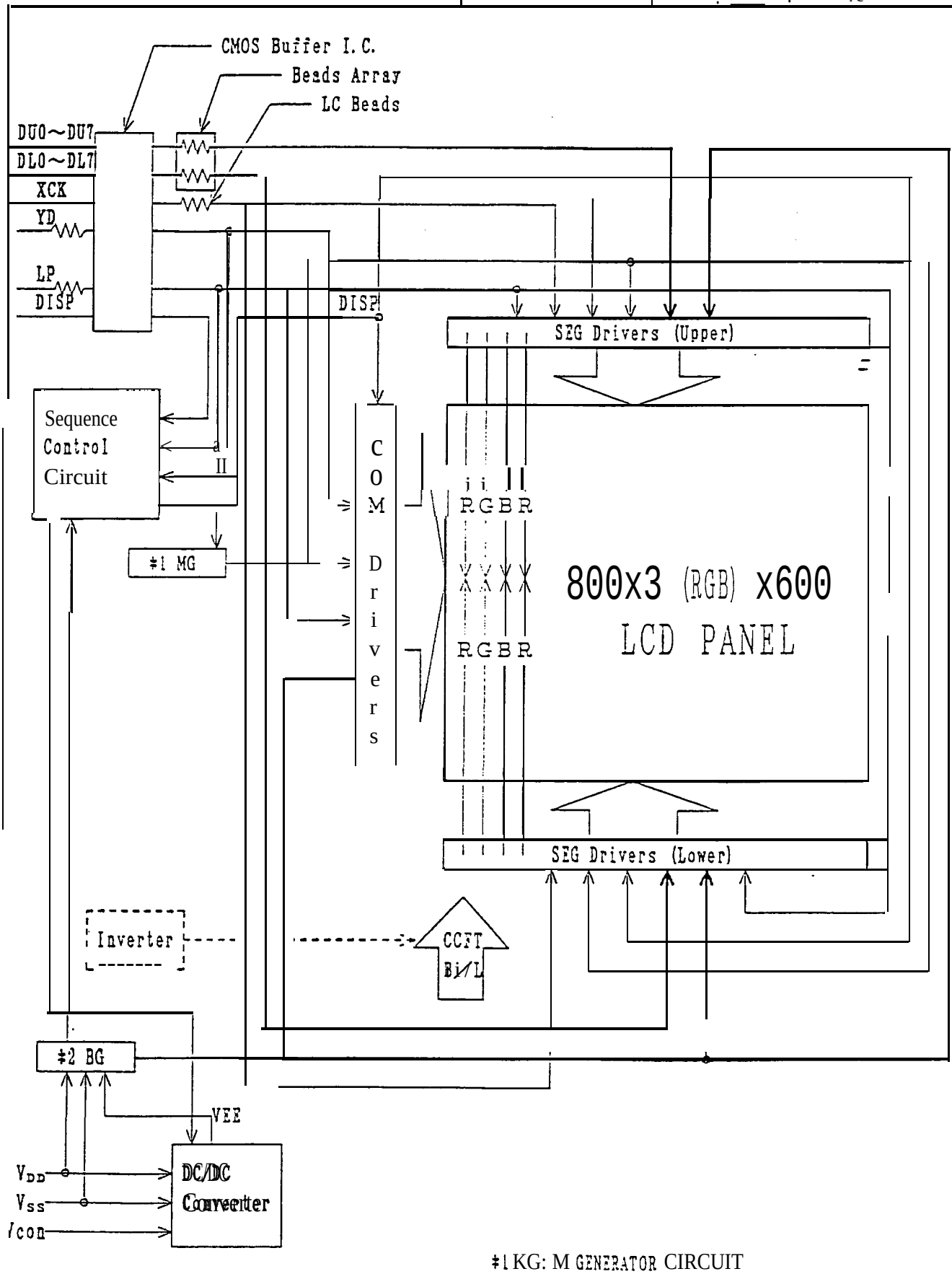


Fig. 9 Circuit block diagram

#1 KG: M GENERATOR CIRCUIT
#2 BG: BIAS GENERATOR & PROTECTION CIRCUIT

8. Characteristics of Backlight

The ratings are given on condition that the following conditions are satisfied,

1) Rating (Note)

Parameter	Frame Frequency	Min	Typ	Max	Unit
Brightness	73 Hz	45	60	—	cd/m²
	120 Hz	50	70	—	cd/m²

2) Measurement circuit: CXA-M10L (TDK) (at IL=6.0 mArms)

3) Measurement equipment: BM-7 (TOPCON Corporation)

4) Measurement conditions

4-1 Measurement circuit voltage: DC=10.4 V, at primary side

4-2 LCD: All digits WHITE, V_{DD}= 5 V, Vcom-Vss=Vmax, DU0～7='H' (WHITE), DL0～7='H' (WHITE)

4-3 Ambient temperature: 25 °C

Measurement shall be executed 30 minutes after turning on.

5) Used lamp: HMBS26D10W245C/X HARISON ELECTRIC CO., LTD. : 1 pc

Cable : UL3239, AWG22 NISSEI ELECTLIC., LTD

5-1 Rating

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remark
Lamp voltage	V_L	-	500	-	Vrms	-
Lamp current	I_L	2.0	5.0	6.0	mArms	(※1)
Lamp power consumption	P_L	-	2.5	-	W	(※2)
Lamp frequency	F_L	20	-	50	kHz	—
Kick-off voltage	V_S	-	-	900	Vrms	Ta=25°C
		-	-	1100	Vrms	Ta=0°C (※3)
Lamp life time	L_L	10000	-	-	h	(※4) (※5)

Within no conductor closed, (CCFT only)

(※1) It is recommended that I_L be not more than 6.0 mArms so that heat radiation of CCFT backlight may least affect the display quality.

(*2) Power consumption excluded inverter loss.

(*3) The circuit voltage (V_S) of the inverter should be designed to have some margin (reference value: 1450 VrmsMIN), because VS may be increased due to the leak current in case of the LCD unit,

(※4) The Lamp life time (L_L) is 10 000 hours at 6.0 mArmsMAX.

(※5) Average life time of CCFT will be decreased when LCD is operating at lower temperature

5-2 Operating life

The operating life time is 10 000 hours or more at 6.0 mArmsMAX.
(Operating life with CXA-M10L-L or. equivalent,)
The inverter should meet the following conditions to keep the specified life time of used lamp;
-Sine, symmetric waveform without spike in positive and negative,
-Output frequency range: 20 KHz～50 KHz
Make sure the operating conditions by executing the burn-in enough time

The operating life time is defined as having ended when any of the following conditions occur; 25±1°C

-When the voltage required for initial discharge has reached 110 % of the initial value

-When the illuminence or quantity of light has decreased to 50 % of the initial value

(NOTE) Rating are defined as the average brightness inside the viewing area specified in Fig. 11.

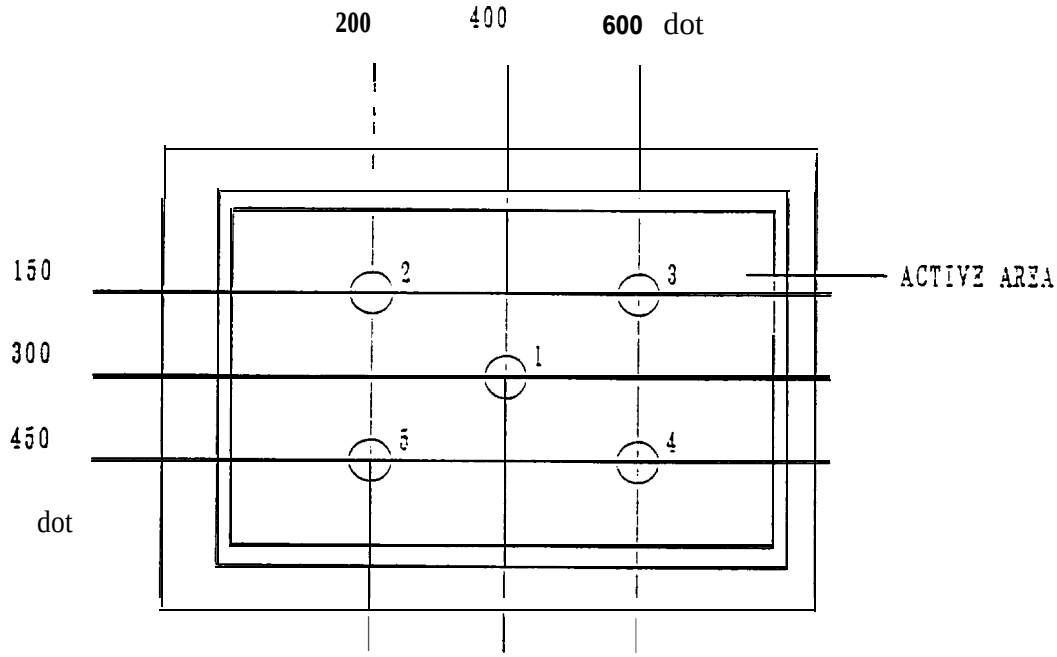
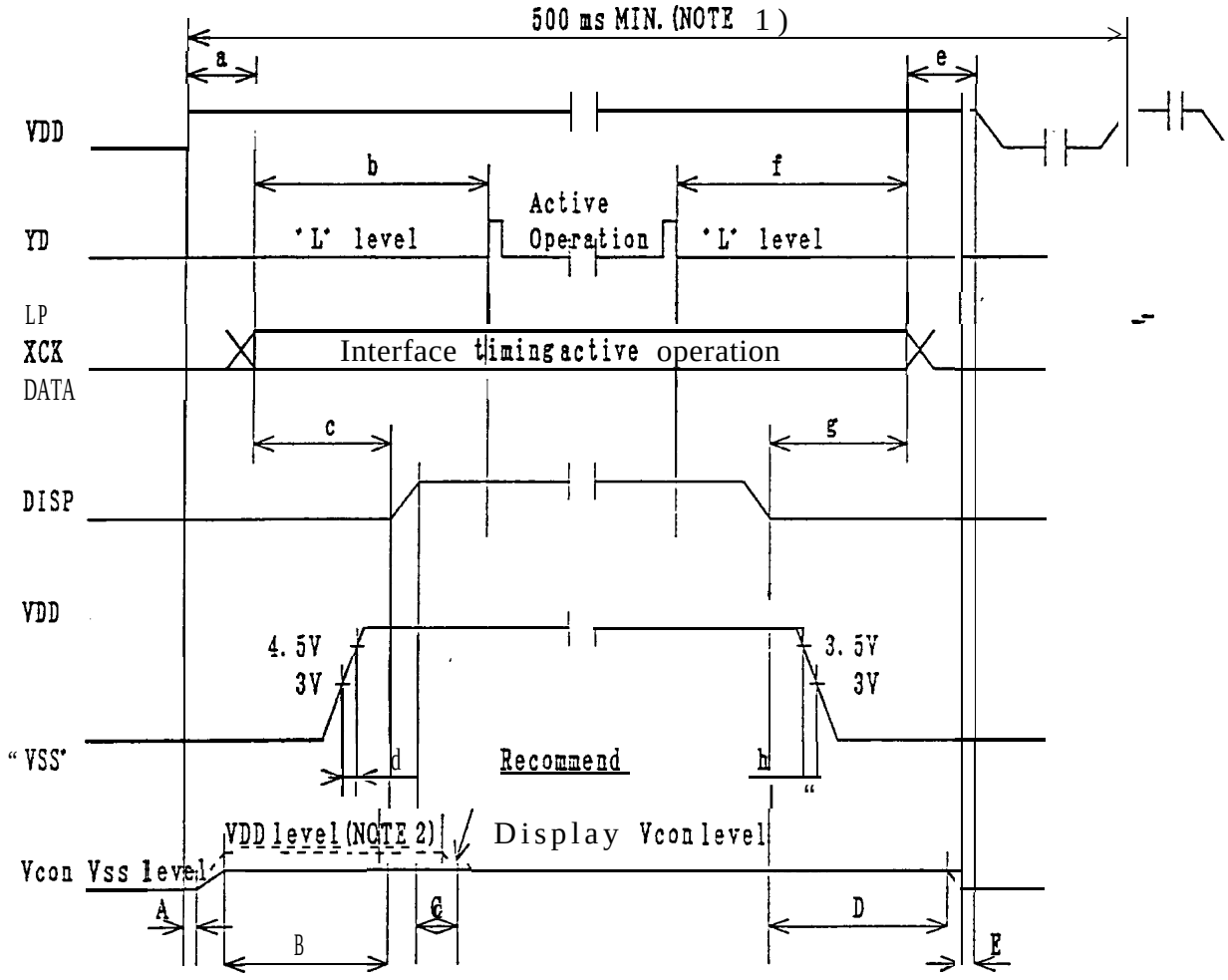


Fig. 11 Measureing points (1~5)

Supplt voltage sequence condition



	POWER ON	
SYMBOL	Allowable value	
a	0 ms MIN.	1 s MAX.
b	0 ms MIN.	1 s MAX.
c	LP×310 MIN.	1 s MAX.
d	–	25ms MAX.
A	0 ms MIN.	–
B	0 ms MIN.	–
C	60ms MIN. (NOTE 2) Recommend	

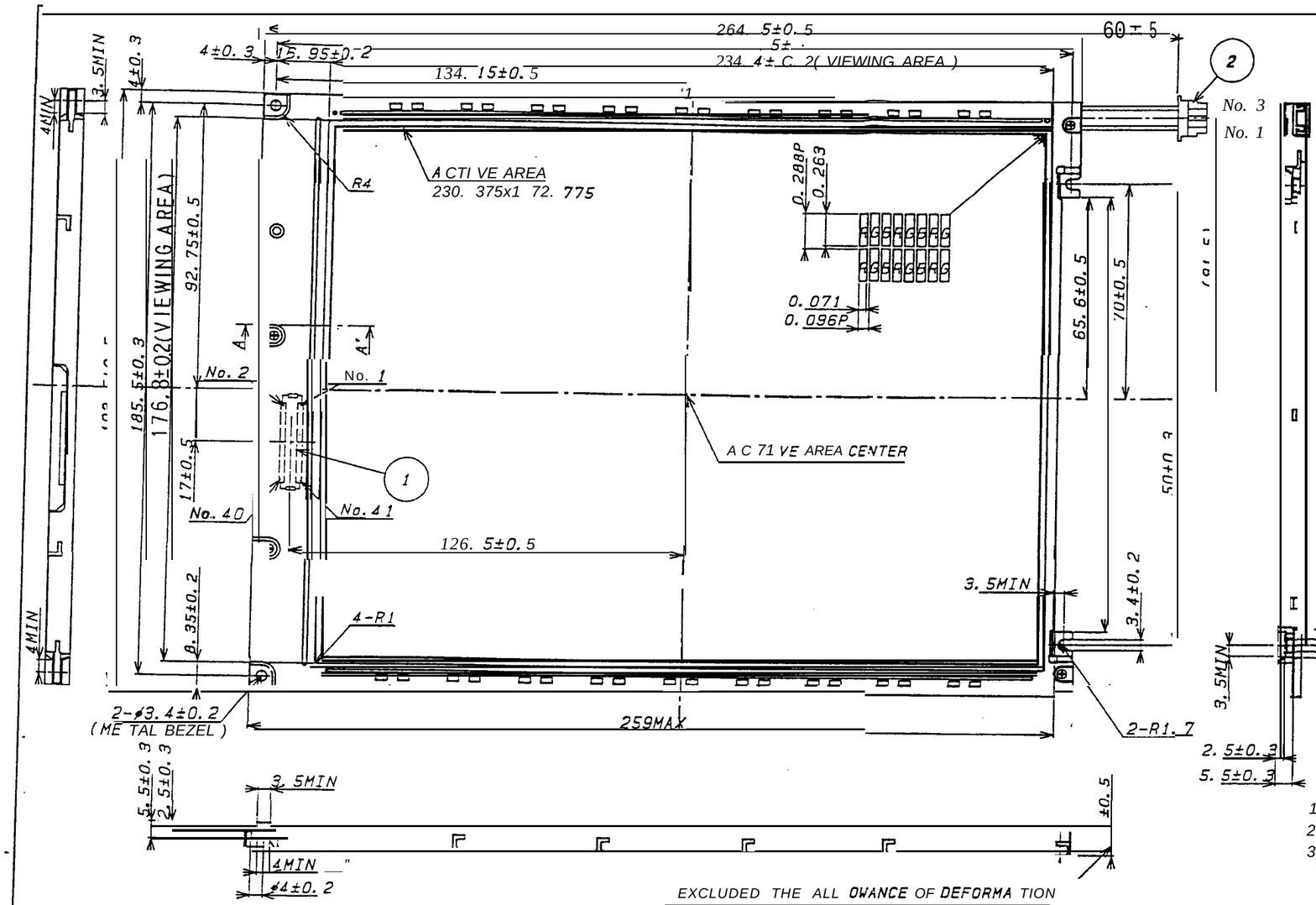
	POWER OFF	
SYMBOL	Allowable value	
e	0 ms MIN.	1 s MAX.
f	0 ms MIN.	–
g	0 ms MIN.	1 s MAX.
h	1 ms MIN.	–
D	0 ms MIN.	–
E	0 ms MIN.	–

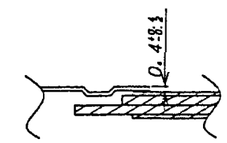
(NOTE 1) Power ON/OFF cycle time. All signals and power line shall be n accordance with above sequence in case of power ON/OFF,

(NOTE 2) In order to reduce the rush current, It is recommended that 'Vcon' to be set to ● VDD' level after power on. C (60ms MIN.) is recommended,

LC95Z54

LM80C20PX



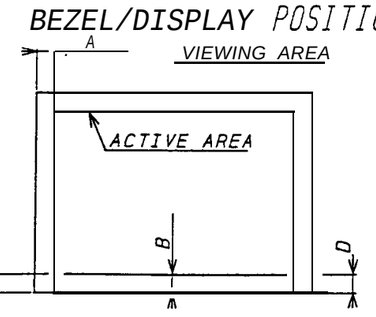


2 CCFT CONNECTOR
JST BHR-03VS-1

Pin 'L AYOUT(3Pin)

1	2	3
HV	NC.	GND

BEZEL/DISPLAY POSITION



1) TOLERANCE X-DIRECTION A :2. 050.5
2) TOLERANCE Y-DIRECTION A :2.0±0.5
3) OBLIQUITY DF DISPLAY AREA | C-D | <0.5

UNSPECIFIED TOL TO BE±0. 5

0' INTERFACE CONNECTOR DF9B-41P-1V(HIROSE)

PIN LA YOU T(41Pin)

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
GND	XCK	GND	GND	1P	YD	GND	GND	Vcc	DISP	GND	GND	GND	DL 7	DL6
16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
DL 5	DL 4	DL 3	DL2	DL 1	DL O	GND	GND	GND	DU0	DU1	DU2	DU3	DU4	DU5
31	32	33	34	35	36	37	38	39	40	41				
DU6	DU7	GND	GNO	GND	VCC	VCC	VCON	Nc	GND	GND				

A	19.					名称 NAME	LCD UNIT OUTLINE DIMENSIONS
A	19.						800xRGBx600DOTS 1/300DUTY
年月日 Dat	訂正記事 Rivise		製No	指当 Prepa	適用機種 odel	部品コード	
材質	板厚				尺度 /		
Design	Trace	Check	Check	Approve	シャープ株式会社 SHARP CORPORATION	作成日付	1995・Sep・29
Ma Jan?		H Kasamatsu			第6部門 デューティー開発センター第二技術課	図番 Drawing No.	ODITRIAVIA7152